**TABLE 13-2: PIC16F87X INSTRUCTION SET**

<table>
<thead>
<tr>
<th>Mnemonic, Operands</th>
<th>Description</th>
<th>Cycles</th>
<th>14-Bit Opcode</th>
<th>Status Affected</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>BYTE-ORIENTED FILE REGISTER OPERATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADDWF f, d</td>
<td>Add W and f</td>
<td>1</td>
<td>00 0111 dfff ffff</td>
<td>C,DC,Z</td>
<td>1.2</td>
</tr>
<tr>
<td>ANDWF f, d</td>
<td>AND W with f</td>
<td>1</td>
<td>00 0101 dfff ffff</td>
<td>Z</td>
<td>1.2</td>
</tr>
<tr>
<td>CLRWF</td>
<td>Clear f</td>
<td>1</td>
<td>00 0001 1fff ffff</td>
<td>Z</td>
<td>2</td>
</tr>
<tr>
<td>COMWF</td>
<td>Clear W</td>
<td>1</td>
<td>00 0001 0fff ffff</td>
<td>Z</td>
<td></td>
</tr>
<tr>
<td>DECF</td>
<td>Decrement f</td>
<td>1</td>
<td>00 0011 dfff ffff</td>
<td>Z</td>
<td>1.2</td>
</tr>
<tr>
<td>DECFSZ</td>
<td>Decrement f, Skip if 0</td>
<td>1(2)</td>
<td>00 1011 dfff ffff</td>
<td>Z</td>
<td>1.2,3</td>
</tr>
<tr>
<td>INCWF</td>
<td>Increment f</td>
<td>1</td>
<td>00 1010 dfff ffff</td>
<td>Z</td>
<td>1.2</td>
</tr>
<tr>
<td>INCFSZ</td>
<td>Increment f, Skip if 0</td>
<td>1(2)</td>
<td>00 1111 dfff ffff</td>
<td>Z</td>
<td>1.2,3</td>
</tr>
<tr>
<td>IORWF f, d</td>
<td>Inclusive OR W with f</td>
<td>1</td>
<td>00 0100 dfff ffff</td>
<td>Z</td>
<td>1.2</td>
</tr>
<tr>
<td>MOVWF f, d</td>
<td>Move f</td>
<td>1</td>
<td>00 1000 dfff ffff</td>
<td>Z</td>
<td>1.2</td>
</tr>
<tr>
<td>MOVWF f, t</td>
<td>Move W to f</td>
<td>1</td>
<td>00 0000 1fff ffff</td>
<td>Z</td>
<td>1.2</td>
</tr>
<tr>
<td>NOP</td>
<td>-</td>
<td>-</td>
<td>00 0000 0000 0000</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>RLF f, d</td>
<td>Rotate Left f through Carry</td>
<td>1</td>
<td>00 1101 dfff ffff</td>
<td>C</td>
<td>1.2</td>
</tr>
<tr>
<td>RRF f, d</td>
<td>Rotate Right f through Carry</td>
<td>1</td>
<td>00 1100 dfff ffff</td>
<td>C</td>
<td>1.2</td>
</tr>
<tr>
<td>SUBWF f, d</td>
<td>Subtract W from f</td>
<td>1</td>
<td>00 0010 dfff ffff</td>
<td>C,DC,Z</td>
<td>1.2</td>
</tr>
<tr>
<td>SWAPF f, d</td>
<td>Swap nibbles in f</td>
<td>1</td>
<td>00 1110 dfff ffff</td>
<td>Z</td>
<td>1.2</td>
</tr>
<tr>
<td>XORWF f, d</td>
<td>Exclusive OR W with f</td>
<td>1</td>
<td>00 0110 dfff ffff</td>
<td>Z</td>
<td>1.2</td>
</tr>
<tr>
<td><strong>BIT-ORIENTED FILE REGISTER OPERATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BCF f, b</td>
<td>Bit Clear f</td>
<td>1</td>
<td>01 00bb bfff ffff</td>
<td>-</td>
<td>1.2</td>
</tr>
<tr>
<td>BSF f, b</td>
<td>Bit Set f</td>
<td>1</td>
<td>01 01bb bfff ffff</td>
<td>-</td>
<td>1.2</td>
</tr>
<tr>
<td>BTFSC f, b</td>
<td>Bit Test f, Skip if Clear</td>
<td>1(2)</td>
<td>01 10bb bfff ffff</td>
<td>-</td>
<td>3</td>
</tr>
<tr>
<td>BTFSS f, b</td>
<td>Bit Test f, Skip if Set</td>
<td>1(2)</td>
<td>01 11bb bfff ffff</td>
<td>-</td>
<td>3</td>
</tr>
<tr>
<td><strong>LITERAL AND CONTROL OPERATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADDLW k</td>
<td>Add literal and W</td>
<td>1</td>
<td>11 111x kkkk kkkk</td>
<td>C,DC,Z</td>
<td>2</td>
</tr>
<tr>
<td>ANDLW k</td>
<td>AND literal with W</td>
<td>1</td>
<td>11 11001 kkkk kkkk</td>
<td>Z</td>
<td>2</td>
</tr>
<tr>
<td>CALL k</td>
<td>Call subroutine</td>
<td>2</td>
<td>10 0kkk kkkk kkkk</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLRWDT</td>
<td>Clear Watchdog Timer</td>
<td>1</td>
<td>00 0000 0120 1000</td>
<td>TO,PD</td>
<td></td>
</tr>
<tr>
<td>GOTO</td>
<td>Go to address</td>
<td>2</td>
<td>10 1kkk kkkk kkkk</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IORLW k</td>
<td>Inclusive OR literal with W</td>
<td>1</td>
<td>11 1100 kkkk kkkk</td>
<td>Z</td>
<td></td>
</tr>
<tr>
<td>MOVLW k</td>
<td>Move literal to W</td>
<td>1</td>
<td>11 00xx kkkk kkkk</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RETFIE</td>
<td>Return from interrupt</td>
<td>2</td>
<td>00 0000 0000 1001</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>RETLW k</td>
<td>Return with literal in W</td>
<td>2</td>
<td>11 01xx kkkk kkkk</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RETURN</td>
<td>Return from Subroutine</td>
<td>2</td>
<td>00 0000 0000 1000</td>
<td>TO,PD</td>
<td></td>
</tr>
<tr>
<td>SLEEP</td>
<td>Go into standby mode</td>
<td>1</td>
<td>00 0000 0110 0011</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>SUBLW k</td>
<td>Subtract W from literal</td>
<td>1</td>
<td>11 110x kkkk kkkk</td>
<td>C,DC,Z</td>
<td>2</td>
</tr>
<tr>
<td>XORLW k</td>
<td>Exclusive OR literal with W</td>
<td>1</td>
<td>11 1010 kkkk kkkk</td>
<td>Z</td>
<td>2</td>
</tr>
</tbody>
</table>

**Note 1:** When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

**Note 2:** If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

**Note 3:** If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOF.

**Note:** Additional information on the mid-range instruction set is available in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023).
### FIGURE 2-3: PIC16F877/876 REGISTER FILE MAP

<table>
<thead>
<tr>
<th>Address</th>
<th>Indirect addr.(†)</th>
<th>File Address</th>
<th>Indirect addr.(†)</th>
<th>File Address</th>
<th>Indirect addr.(†)</th>
<th>File Address</th>
<th>Indirect addr.(†)</th>
<th>File Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>TMRO</td>
<td>100h</td>
<td>OPTION_REG</td>
<td>101h</td>
<td>TMRO</td>
<td>100h</td>
<td>OPTION_REG</td>
<td>180h</td>
</tr>
<tr>
<td>01h</td>
<td>PCL</td>
<td>102h</td>
<td>PCL</td>
<td>103h</td>
<td>PCL</td>
<td>104h</td>
<td>TRISB</td>
<td>186h</td>
</tr>
<tr>
<td>02h</td>
<td>STATUS</td>
<td>105h</td>
<td>STATUS</td>
<td>106h</td>
<td>PORTB</td>
<td>107h</td>
<td>TRISB</td>
<td>187h</td>
</tr>
<tr>
<td>03h</td>
<td>FSR</td>
<td>108h</td>
<td>FSR</td>
<td>109h</td>
<td>PORTC</td>
<td>110h</td>
<td>TRISB</td>
<td>188h</td>
</tr>
<tr>
<td>04h</td>
<td>PORTA</td>
<td>111h</td>
<td>TRISA</td>
<td>112h</td>
<td>PORTC</td>
<td>113h</td>
<td>TRISB</td>
<td>189h</td>
</tr>
<tr>
<td>05h</td>
<td>PORTB</td>
<td>114h</td>
<td>TRISB</td>
<td>115h</td>
<td>PORTD1</td>
<td>116h</td>
<td>TRISB</td>
<td>189h</td>
</tr>
<tr>
<td>06h</td>
<td>PORTC</td>
<td>117h</td>
<td>TRISB</td>
<td>118h</td>
<td>PORTE1</td>
<td>119h</td>
<td>TRISB</td>
<td>189h</td>
</tr>
<tr>
<td>07h</td>
<td>PORTD1</td>
<td>120h</td>
<td>TRISB</td>
<td>121h</td>
<td>PORTE1</td>
<td>122h</td>
<td>TRISB</td>
<td>189h</td>
</tr>
<tr>
<td>08h</td>
<td>PORTE1</td>
<td>123h</td>
<td>TRISB</td>
<td>124h</td>
<td>PORTE1</td>
<td>125h</td>
<td>TRISB</td>
<td>189h</td>
</tr>
<tr>
<td>09h</td>
<td>PCLATH</td>
<td>126h</td>
<td>PCLATH</td>
<td>127h</td>
<td>PCLATH</td>
<td>128h</td>
<td>PCLATH</td>
<td>18Ah</td>
</tr>
<tr>
<td>0Ah</td>
<td>INTCON</td>
<td>129h</td>
<td>INTCON</td>
<td>130h</td>
<td>INTCON</td>
<td>131h</td>
<td>INTCON</td>
<td>18Bh</td>
</tr>
<tr>
<td>0Bh</td>
<td>PIR1</td>
<td>132h</td>
<td>EEDATA</td>
<td>133h</td>
<td>EEDATA</td>
<td>134h</td>
<td>EEDATA</td>
<td>18Ch</td>
</tr>
<tr>
<td>0Ch</td>
<td>PIE1</td>
<td>135h</td>
<td>EEDATA</td>
<td>136h</td>
<td>EEDATA</td>
<td>137h</td>
<td>EEDATA</td>
<td>18Dh</td>
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<tr>
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<td>PIE2</td>
<td>138h</td>
<td>EEDATA</td>
<td>139h</td>
<td>EEDATA</td>
<td>140h</td>
<td>EEDATA</td>
<td>18Dh</td>
</tr>
<tr>
<td>0Eh</td>
<td>TMR1L</td>
<td>141h</td>
<td>TMR1L</td>
<td>142h</td>
<td>Reserved</td>
<td>18Eh</td>
<td>Reserved</td>
<td>18Eh</td>
</tr>
<tr>
<td>0Fh</td>
<td>TMR1H</td>
<td>143h</td>
<td>TMR1H</td>
<td>144h</td>
<td>Reserved</td>
<td>18Fh</td>
<td>Reserved</td>
<td>18Fh</td>
</tr>
<tr>
<td>10h</td>
<td>T1CON</td>
<td>145h</td>
<td>T1CON</td>
<td>146h</td>
<td>110h</td>
<td>147h</td>
<td>110h</td>
<td>190h</td>
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<tr>
<td>11h</td>
<td>TMR2</td>
<td>111h</td>
<td>TMR2</td>
<td>112h</td>
<td>111h</td>
<td>113h</td>
<td>111h</td>
<td>191h</td>
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<td>12h</td>
<td>T2CON</td>
<td>114h</td>
<td>T2CON</td>
<td>115h</td>
<td>114h</td>
<td>116h</td>
<td>114h</td>
<td>192h</td>
</tr>
<tr>
<td>13h</td>
<td>SSPBUF</td>
<td>117h</td>
<td>SSPBUF</td>
<td>118h</td>
<td>117h</td>
<td>119h</td>
<td>117h</td>
<td>193h</td>
</tr>
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<td>14h</td>
<td>SSPCON</td>
<td>119h</td>
<td>SSPCON</td>
<td>120h</td>
<td>119h</td>
<td>121h</td>
<td>119h</td>
<td>194h</td>
</tr>
<tr>
<td>15h</td>
<td>CCP1CON</td>
<td>122h</td>
<td>CCP1CON</td>
<td>123h</td>
<td>122h</td>
<td>124h</td>
<td>122h</td>
<td>195h</td>
</tr>
<tr>
<td>16h</td>
<td>CCP1CON</td>
<td>125h</td>
<td>CCP1CON</td>
<td>126h</td>
<td>125h</td>
<td>127h</td>
<td>125h</td>
<td>196h</td>
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<td>17h</td>
<td>RXSTA</td>
<td>128h</td>
<td>RXSTA</td>
<td>129h</td>
<td>128h</td>
<td>130h</td>
<td>128h</td>
<td>197h</td>
</tr>
<tr>
<td>18h</td>
<td>TXREG</td>
<td>131h</td>
<td>TXREG</td>
<td>132h</td>
<td>131h</td>
<td>133h</td>
<td>131h</td>
<td>198h</td>
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<tr>
<td>19h</td>
<td>RCREG</td>
<td>134h</td>
<td>RCREG</td>
<td>135h</td>
<td>134h</td>
<td>136h</td>
<td>134h</td>
<td>199h</td>
</tr>
<tr>
<td>1Ah</td>
<td>SPBRG</td>
<td>137h</td>
<td>SPBRG</td>
<td>138h</td>
<td>137h</td>
<td>139h</td>
<td>137h</td>
<td>19Ah</td>
</tr>
<tr>
<td>1Bh</td>
<td>CCP2L</td>
<td>140h</td>
<td>CCP2L</td>
<td>141h</td>
<td>140h</td>
<td>142h</td>
<td>140h</td>
<td>19Bh</td>
</tr>
<tr>
<td>1Ch</td>
<td>CCP2H</td>
<td>143h</td>
<td>CCP2H</td>
<td>144h</td>
<td>143h</td>
<td>145h</td>
<td>143h</td>
<td>19Ch</td>
</tr>
<tr>
<td>1Dh</td>
<td>CCP2CON</td>
<td>146h</td>
<td>CCP2CON</td>
<td>147h</td>
<td>146h</td>
<td>148h</td>
<td>146h</td>
<td>19Dh</td>
</tr>
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<td>149h</td>
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<td>150h</td>
<td>149h</td>
<td>151h</td>
<td>149h</td>
<td>19Eh</td>
</tr>
<tr>
<td>1Fh</td>
<td>ADCON0</td>
<td>152h</td>
<td>ADCON0</td>
<td>153h</td>
<td>152h</td>
<td>154h</td>
<td>152h</td>
<td>19Fh</td>
</tr>
</tbody>
</table>

General Purpose Register
96 Bytes

Bank 0
7Fh

Bank 1
0Fh

Bank 2
FFh

Bank 3
1FFh

General Purpose Register
80 Bytes

Accesses 70h-7Fh

General Purpose Register
16 Bytes

Accesses 16Fh-170h

General Purpose Register
16 Bytes

Accesses 1EFh-1FFh

General Purpose Register
80 Bytes

Accesses 17Fh-170h

General Purpose Register
80 Bytes

Accesses 00h-0Fh

Unimplemented data memory locations, read as '0'.
* Not a physical register.

**Note 1:** These registers are not implemented on the PIC16F876.

**Note 2:** These registers are reserved, maintain these registers clear.
TABLE 5-1: REGISTERS ASSOCIATED WITH TIMER0

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on: POR, BOR</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>01h, 10h</td>
<td>TMR0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xxxxx xxxxx</td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>0Bh, 8Bh, 10Bh, 18Bh</td>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TOIE</td>
<td>INTOE</td>
<td>RBIE</td>
<td>TOIF</td>
<td>INTF</td>
<td>RBIF</td>
<td>0000 000x</td>
<td>0000 000u</td>
</tr>
<tr>
<td>81h, 18h</td>
<td>OPTION_REG</td>
<td>RBPU</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
<td>1111 1111</td>
<td>1111 1111</td>
</tr>
</tbody>
</table>

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

Figure 11-1: Timer0 Block Diagram

Note 1: T0CS, T0SE, PSA, PS2:PS0 (OPTION_REG<5:0>).
Note 2: The prescaler is shared with Watchdog Timer (refer to Figure 11-6 for detailed block diagram).

TABLE 6-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on: POR, BOR</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0Bh, 8Bh, 10Bh, 18Bh</td>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TOIE</td>
<td>INTOE</td>
<td>RBIE</td>
<td>TOIF</td>
<td>INTF</td>
<td>RBIF</td>
<td>0000 000x</td>
<td>0000 000u</td>
</tr>
<tr>
<td>0Ch</td>
<td>PIR1</td>
<td>PSPIE</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSPIF</td>
<td>CCP1F</td>
<td>TMRI2F</td>
<td>TMRI1F</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>8Ch</td>
<td>PIE1</td>
<td>PSPIE</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSPIE</td>
<td>CCP1IE</td>
<td>TMRI2IE</td>
<td>TMRI1IE</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>0Eh</td>
<td>TMRI1L</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xxxx xxxx</td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>0Fh</td>
<td>TMRI1H</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xxxx xxxx</td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>10h</td>
<td>T1CON</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>--00 0000</td>
<td>--00 uuuu</td>
</tr>
</tbody>
</table>

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.
Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F873/876; always maintain these bits clear.

Figure 12-1: Timer1 Block Diagram

Note 1: When the T1OSCEN bit is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.
Section 11. Timer0

11.2 Control Register

The OPTION_REG register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the External INT Interrupt, TMRO, and the weak pull-ups on PORTB.

**Note:** To achieve a 1:1 prescaler assignment for the TMRO register, assign the prescaler to the Watchdog Timer.

Register 11-1: OPTION_REG Register

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>RBPU (1)</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
</tr>
</tbody>
</table>

bit 7  **RBPU (1):** Weak Pull-up Enable bit
1 = Weak pull-ups are disabled
0 = Weak pull-ups are enabled by individual port latch values

bit 6  **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of INT pin
0 = Interrupt on falling edge of INT pin

bit 5  **T0CS:** TMR0 Clock Source Select bit
1 = Transition on TOCKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4  **T0SE:** TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on TOCKI pin
0 = Increment on low-to-high transition on TOCKI pin

bit 3  **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2:0  **PS2:PS0:** Prescaler Rate Select bits

<table>
<thead>
<tr>
<th>Bit Value</th>
<th>TMRO Rate</th>
<th>WDT Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>1 : 2</td>
<td>1 : 1</td>
</tr>
<tr>
<td>001</td>
<td>1 : 4</td>
<td>1 : 2</td>
</tr>
<tr>
<td>010</td>
<td>1 : 8</td>
<td>1 : 4</td>
</tr>
<tr>
<td>011</td>
<td>1 : 16</td>
<td>1 : 8</td>
</tr>
<tr>
<td>100</td>
<td>1 : 32</td>
<td>1 : 16</td>
</tr>
<tr>
<td>101</td>
<td>1 : 64</td>
<td>1 : 32</td>
</tr>
<tr>
<td>110</td>
<td>1 : 128</td>
<td>1 : 64</td>
</tr>
<tr>
<td>111</td>
<td>1 : 256</td>
<td>1 : 128</td>
</tr>
</tbody>
</table>

**Legend**
R = Readable bit  W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

**Note 1:** Some devices call this bit GPPU. Devices that have the RBPU bit, have the weak pull-ups on PORTB, while devices that have the GPPU have the weak pull-ups on the GPIO Port.
12.2 Control Register

Register 12-1 shows the Timer1 control register.

**Register 12-1: T1CON: Timer1 Control Register**

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>T1CKPS1</td>
<td>T1CKPS0</td>
<td>T1OSCEN</td>
<td>T1SYNC</td>
<td>TMR1CS</td>
<td>TMR1ON</td>
</tr>
</tbody>
</table>

bit 7

bit 6:3 | Unimplemented: Read as '0'

bit 5:4 | T1CKPS1: T1CKPS0: Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3 | T1OSCEN: Timer1 Oscillator Enable bit
1 = Oscillator is enabled
0 = Oscillator is shut off. The oscillator inverter and feedback resistor are turned off to eliminate power drain

bit 2 | T1SYNC: Timer1 External Clock Input Synchronization Select bit
When TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
When TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1 | TMR1CS: Timer1 Clock Source Select bit
1 = External clock from pin T1OSO/T1CKI (on the rising edge)
0 = Internal clock (Fosc/4)

bit 0 | TMR1ON: Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

Legend
R = Readable bit  W = Writable bit
U = Unimplemented bit, read as ‘0’  - n = Value at POR reset
FIGURE 7-1: TIMER2 BLOCK DIAGRAM

Note 1: TMR2 register output can be software selected by the SSP module as a baud clock.

TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on: POR, BOR</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0Bh, 0Dh, 10Bh, 18Bh</td>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>RBIE</td>
<td>T0IF</td>
<td>INTF</td>
<td>RBIF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>0Ch</td>
<td>PIR1</td>
<td>ADIF</td>
<td>ADIE</td>
<td>T0IF</td>
<td>RCIF</td>
<td>SSIF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>8Ch</td>
<td>PIR2</td>
<td>ADIE</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIF</td>
<td>SSIE</td>
<td>CCP1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>11h</td>
<td>TMR2</td>
<td>Timer2 Module’s Register</td>
<td>0000 0000</td>
<td>0000 0000</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12h</td>
<td>T2CON</td>
<td>TOUTPS3</td>
<td>TOUTPS2</td>
<td>TOUTPS1</td>
<td>TOUTPS0</td>
<td>TMR2ON</td>
<td>T2CKPS1</td>
<td>T2CKPS0</td>
<td>-000 0000</td>
<td>-000 0000</td>
<td></td>
</tr>
<tr>
<td>92h</td>
<td>PR2</td>
<td>Timer2 Period Register</td>
<td>1111 1111</td>
<td>1111 1111</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer2 module.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F873/878; always maintain these bits clear.

REGISTER 7-1: T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)

<table>
<thead>
<tr>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TOUTPS3</td>
<td>TOUTPS2</td>
<td>TOUTPS1</td>
<td>TOUTPS0</td>
<td>TMR2ON</td>
<td>T2CKPS1</td>
<td>T2CKPS0</td>
<td></td>
</tr>
</tbody>
</table>

bit 7

Unimplemented: Read as '0'

bit 6-3

TOUTPS3:TOUTPS0: Timer2 Output Postscale Select bits

0000 = 1:1 Postscale
0001 = 1:2 Postscale
0010 = 1:3 Postscale
0011 = 1:4 Postscale
...
1111 = 1:16 Postscale

bit 2

TMR2ON: Timer2 On bit

1 = Timer2 is on
0 = Timer2 is off

bit 1-0

T2CKPS1:T2CKPS0: Timer2 Clock Prescale Select bits

00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16
Register 3-2: STATUS Register

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R-1</th>
<th>R-1</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRP</td>
<td>RP1</td>
<td>RP0</td>
<td>TO</td>
<td>PD</td>
<td>Z</td>
<td>DC</td>
<td>C</td>
</tr>
</tbody>
</table>

bit 7
IRP: Register Bank Select bit (used for indirect addressing)
1 = Bank 2, 3 (100h - 1FFh)
0 = Bank 0, 1 (00h - FFh)
For devices with only Bank0 and Bank1 the IRP bit is reserved, always maintain this bit clear.

bit 6:5
RP1:RP0: Register Bank Select bits (used for direct addressing)
11 = Bank 3 (180h - 1FFh)
10 = Bank 2 (100h - 17Fh)
01 = Bank 1 (80h - FFh)
00 = Bank 0 (00h - 7Fh)
Each bank is 128 bytes. For devices with only Bank0 and Bank1 the IRP bit is reserved, always maintain this bit clear.

bit 4
TO: Time-out bit
1 = After power-up, CLRWDY instruction, or SLEEP instruction
0 = A WDT time-out occurred

bit 3
PD: Power-down bit
1 = After power-up or by the CLRWDY instruction
0 = By execution of the SLEEP instruction

bit 2
Z: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

Register 3-1: PCON Register

<table>
<thead>
<tr>
<th>R-u</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPEEN</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>PER</td>
<td>POR</td>
<td>BOR</td>
</tr>
</tbody>
</table>

bit 7
MPEEN: Memory Parity Error Circuitry Status bit
This bit reflects the value of the MPEEN configuration bit.

bit 6:3
Unimplemented: Read as '0'

bit 2
PER: Memory Parity Error Reset Status bit
1 = No parity error reset occurred
0 = A program memory fetch parity error occurred
   (must be set in software after a Power-on Reset or Parity Error Reset occurs)

bit 1
POR: Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0
BOR: Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset or Power-on Reset occurs)

Table 3-2: Status Bits and Their Significance

<table>
<thead>
<tr>
<th>POR</th>
<th>BOR(1)</th>
<th>TO</th>
<th>PD</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>x</td>
<td>1</td>
<td>1</td>
<td>Power-on Reset</td>
</tr>
<tr>
<td>0</td>
<td>x</td>
<td>0</td>
<td>x</td>
<td>Illegal, TO is set on POR</td>
</tr>
<tr>
<td>0</td>
<td>x</td>
<td>x</td>
<td>0</td>
<td>Illegal, PD is set on POR</td>
</tr>
<tr>
<td>1(2)</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Brown-out Reset</td>
</tr>
<tr>
<td>1(2)</td>
<td>1(2)</td>
<td>0</td>
<td>1</td>
<td>WDT Reset</td>
</tr>
<tr>
<td>1(2)</td>
<td>1(2)</td>
<td>0</td>
<td>0</td>
<td>WDT Wake-up</td>
</tr>
<tr>
<td>1(2)</td>
<td>1(2)</td>
<td>u</td>
<td>u</td>
<td>MCLR reset during normal operation</td>
</tr>
<tr>
<td>1(2)</td>
<td>1(2)</td>
<td>1</td>
<td>0</td>
<td>MCLR reset during SLEEP</td>
</tr>
</tbody>
</table>

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.
Note 1: Not all devices have BOR circuitry.
Note 2: These bits are unchanged for the given conditions, and when initialized (set) after a POR or a BOR will read as a '1'.


TABLE 10-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on: POR, BOR</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0Bh, 08h, 10Bh, 18Bh</td>
<td>INTO</td>
<td>GIE</td>
<td>PEIE</td>
<td>TOIE</td>
<td>INTE</td>
<td>RBIE</td>
<td>T0IF</td>
<td>INTO</td>
<td>T0IF</td>
<td>R0IF</td>
<td>0000 000x</td>
</tr>
<tr>
<td>0Ch</td>
<td>PIR1</td>
<td>P_SPIF(1)</td>
<td>ADIE</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSPIF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>18h</td>
<td>RCSTA</td>
<td>SPEN</td>
<td>RX9</td>
<td>SREN</td>
<td>CREN</td>
<td>-</td>
<td>FERR</td>
<td>OERR</td>
<td>RX9D</td>
<td>0000 0000 0000 0000 0000 0000</td>
<td></td>
</tr>
<tr>
<td>1Ah</td>
<td>RCREG</td>
<td>USART Receive Register</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>8Ch</td>
<td>PIE1</td>
<td>P_SPIE(1)</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSPIE</td>
<td>CCP1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>98h</td>
<td>TXSTA</td>
<td>CSRC</td>
<td>TX9</td>
<td>TXEN</td>
<td>SYNC</td>
<td>-</td>
<td>BRGH</td>
<td>TRMT</td>
<td>TX9D</td>
<td>0000 0000 0000 0100 0000 0000</td>
<td></td>
</tr>
<tr>
<td>99h</td>
<td>SPBRG</td>
<td>Baud Rate Generator Register</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

FIGURE 10-4: USART RECEIVE BLOCK DIAGRAM

TABLE 10-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on: POR, BOR</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0Bh, 08h, 10Bh, 18Bh</td>
<td>INTO</td>
<td>GIE</td>
<td>PEIE</td>
<td>TOIE</td>
<td>INTE</td>
<td>RBIE</td>
<td>T0IF</td>
<td>INTO</td>
<td>T0IF</td>
<td>R0IF</td>
<td>0000 000x</td>
</tr>
<tr>
<td>0Ch</td>
<td>PIR1</td>
<td>P_SPIF(1)</td>
<td>ADIE</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSPIF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>18h</td>
<td>RCSTA</td>
<td>SPEN</td>
<td>RX9</td>
<td>SREN</td>
<td>CREN</td>
<td>-</td>
<td>FERR</td>
<td>OERR</td>
<td>RX9D</td>
<td>0000 0000 0000 0000 0000 0000</td>
<td></td>
</tr>
<tr>
<td>19h</td>
<td>TXREG</td>
<td>USART Transmit Register</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>8Ch</td>
<td>PIE1</td>
<td>P_SPIE(1)</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSPIE</td>
<td>CCP1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>98h</td>
<td>TXSTA</td>
<td>CSRC</td>
<td>TX9</td>
<td>TXEN</td>
<td>SYNC</td>
<td>-</td>
<td>BRGH</td>
<td>TRMT</td>
<td>TX9D</td>
<td>0000 0000 0000 0100 0000 0000</td>
<td></td>
</tr>
<tr>
<td>99h</td>
<td>SPBRG</td>
<td>Baud Rate Generator Register</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.
Note 1: Bits P_SPIE and P_SPIF are reserved on the PIC16F873/876; always maintain these bits clear.

FIGURE 10-1: USART TRANSMIT BLOCK DIAGRAM
TABLE 10-1: BAUD RATE FORMULA

<table>
<thead>
<tr>
<th>SYNC</th>
<th>BRGH = 0 (Low Speed)</th>
<th>BRGH = 1 (High Speed)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>(Asynchronous) Baud Rate = Fosc/(64(X+1))</td>
<td>Baud Rate = Fosc/(16(X+1))</td>
</tr>
<tr>
<td>1</td>
<td>(Synchronous) Baud Rate = Fosc/(4(X+1))</td>
<td>N/A</td>
</tr>
</tbody>
</table>

X = value in SPBRG (0 to 255)

TABLE 10-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on: POR, BOR</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>98h</td>
<td>TXSTA</td>
<td>CSRC</td>
<td>TX9</td>
<td>TXEN</td>
<td>SYNC</td>
<td></td>
<td>BRGH</td>
<td>TRMT</td>
<td>TX9D</td>
<td>0000 010</td>
<td>0000 010</td>
</tr>
<tr>
<td>18h</td>
<td>RCSTA</td>
<td>SPEN</td>
<td>RX9</td>
<td>SREN</td>
<td>CREN</td>
<td>ADDEN</td>
<td>FERR</td>
<td>OERR</td>
<td>RX9D</td>
<td>0000 000X</td>
<td>0000 000X</td>
</tr>
<tr>
<td>99h</td>
<td>SPBRG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
</tbody>
</table>

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used by the BRG.

REGISTER 10-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER (ADDRESS 98h)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R-1</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSRC</td>
<td>TX9</td>
<td>TXEN</td>
<td>SYNC</td>
<td></td>
<td>BRGH</td>
<td>TRMT</td>
<td>TX9D</td>
</tr>
</tbody>
</table>

bit 7

CSRC: Clock Source Select bit
Asynchronous mode:
Don't care
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6

TX9: 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5

TXEN: Transmit Enable bit
1 = Transmit enabled
0 = Transmit disabled

Note: SREN/CREN overrides TXEN in SYNC mode.

bit 4

SYNC: USART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3

Unimplemented: Read as '0'

bit 2

BRGH: High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed
Synchronous mode:
Unused in this mode

bit 1

TRMT: Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0

TX9D: 9th bit of Transmit Data, can be parity bit

Legend:

R = Readable bit       W = Writable bit       U = Unimplemented bit, read as '0'
-n = Value at POR      '1' = Bit is set       '0' = Bit is cleared           x = Bit is unknown
REGISTER 10-2:  RCSTA: RECEIVE STATUS AND CONTROL REGISTER (ADDRESS 18h)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-X</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPEN</td>
<td>RX9</td>
<td>SREN</td>
<td>CREN</td>
<td>ADDEN</td>
<td>FERR</td>
<td>OERR</td>
<td>RX9D</td>
</tr>
</tbody>
</table>

bit 7  SPEN: Serial Port Enable bit
      1 = Serial port enabled (configures RC7/RX/DT and RC6/TX/CK pins as serial port pins)
      0 = Serial port disabled

bit 6  RX9: 9-bit Receive Enable bit
      1 = Selects 9-bit reception
      0 = Selects 8-bit reception

bit 5  SREN: Single Receive Enable bit
       Asynchronous mode:
       Don’t care
       Synchronous mode - master:
       1 = Enables single receive
       0 = Disables single receive
       This bit is cleared after reception is complete.
       Synchronous mode - slave:
       Don’t care

bit 4  CREN: Continuous Receive Enable bit
       Asynchronous mode:
       1 = Enables continuous receive
       0 = Disables continuous receive
       Synchronous mode:
       1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
       0 = Disables continuous receive

bit 3  ADDEN: Address Detect Enable bit
       Asynchronous mode 9-bit (RX9 = 1):
       1 = Enables address detection, enables interrupt and load of the receive buffer when RSR<8> is set
       0 = Disables address detection, all bytes are received, and ninth bit can be used as parity bit

bit 2  FERR: Framing Error bit
       1 = Framing error (can be updated by reading RCREG register and receive next valid byte)
       0 = No framing error

bit 1  OERR: Overrun Error bit
       1 = Overrun error (can be cleared by clearing bit CREN)
       0 = No overrun error

bit 0  RX9D: 9th bit of Received Data (can be parity bit, but must be calculated by user firmware)

Legend:
R = Readable bit       W = Writable bit       U = Unimplemented bit, read as ‘0’
- n = Value at POR     ’1’ = Bit is set       ’0’ = Bit is cleared       x = Bit is unknown
TABLE 9-3: REGISTERS ASSOCIATED WITH I^2C OPERATION

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on: POR, BOR</th>
<th>Value on: MCLR, WDT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0Ch</td>
<td>PIR1</td>
<td>PSPIF</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSPIF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>0Ch</td>
<td>PIE1</td>
<td>PSPIE</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSPIE</td>
<td>CCP1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>0Dh</td>
<td>PIR2</td>
<td>—</td>
<td>—</td>
<td>(2)</td>
<td>—</td>
<td>EEIF</td>
<td>BCLIF</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>0Dh</td>
<td>PIE2</td>
<td>—</td>
<td>—</td>
<td>(2)</td>
<td>—</td>
<td>EEIF</td>
<td>BCLIE</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>13h</td>
<td>SSPBUF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SyncPort</td>
<td></td>
</tr>
<tr>
<td>14h</td>
<td>SSPCON</td>
<td>WCOL</td>
<td>SSPOV</td>
<td>SSPEN</td>
<td>CKP</td>
<td>SSPM3</td>
<td>SSPM2</td>
<td>SSPM1</td>
<td>SSPM0</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>91h</td>
<td>SSPCON2</td>
<td>GCEN</td>
<td>ACKSTAT</td>
<td>ACKDT</td>
<td>ACKEN</td>
<td>RCEN</td>
<td>PEN</td>
<td>RSEN</td>
<td>SEN</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>93h</td>
<td>SSPADD</td>
<td>I^2C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Addr</td>
<td>0000 0000</td>
</tr>
<tr>
<td>94h</td>
<td>SSPSTAT</td>
<td>SMP</td>
<td>CKE</td>
<td>D/A</td>
<td>P</td>
<td>S</td>
<td>R/W</td>
<td>UA</td>
<td>BF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
</tbody>
</table>

Legend:  x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the SSP in I^2C mode.

Note 1: These bits are reserved on PIC16F873/876 devices; always maintain these bits clear.

Note 2: These bits are reserved on these devices; always maintain these bits clear.
TABLE 9-1: REGISTERS ASSOCIATED WITH SPI OPERATION

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on: POR, BOR</th>
<th>Value on: MCLR, WDT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0Bh, 8Bh, 10Bh, 18Bh</td>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TOIE</td>
<td>INTE</td>
<td>RBIE</td>
<td>T0IF</td>
<td>INTF</td>
<td>RBIF</td>
<td>0000 0000x</td>
<td>0000 0000u</td>
</tr>
<tr>
<td>0Ch</td>
<td>PIE1</td>
<td>PSP1F</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSP1F</td>
<td>CCP1F</td>
<td>TMR1F</td>
<td>TMR1I</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8Ch</td>
<td>PIE1</td>
<td>PSP1E</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSP1E</td>
<td>CCP1E</td>
<td>TMR2E</td>
<td>TMR1IE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13h</td>
<td>SSPBUF</td>
<td>Synchronous Serial Port Receive Buffer/Transmit Register</td>
<td>0000 0000</td>
<td>0000 0000</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14h</td>
<td>SSPCON</td>
<td>WCOL</td>
<td>SSPOV</td>
<td>SSPEN</td>
<td>CKP</td>
<td>SSPM3</td>
<td>SSPM2</td>
<td>SSPM1</td>
<td>SSPM0</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>94h</td>
<td>SSPSTAT</td>
<td>SMP</td>
<td>CKE</td>
<td>D/A</td>
<td>P</td>
<td>S</td>
<td>R/W</td>
<td>UA</td>
<td>BF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
</tbody>
</table>

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the SSP in SPI mode.

Note 1: These bits are reserved on PIC16F873/876 devices; always maintain these bits clear.

REGISTER 4-1: EECON1 REGISTER (ADDRESS 18Ch)

<table>
<thead>
<tr>
<th>R/W-x</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x</th>
<th>R/W-0</th>
<th>R/S-0</th>
<th>R/S-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEPGD</td>
<td></td>
<td></td>
<td></td>
<td>WRERR</td>
<td>WREN</td>
<td>WR</td>
<td>RD</td>
</tr>
</tbody>
</table>

bit 7    EEPGD: Program/Data EEPROM Select bit
         1 = Accesses program memory
         0 = Accesses data memory
         (This bit cannot be changed while a read or write operation is in progress)

bit 6-4  Unimplemented: Read as '0'

bit 3    WRERR: EEPROM Error Flag bit
         1 = A write operation is prematurely terminated
         (any MCLR Reset or any WDT Reset during normal operation)
         0 = The write operation completed

bit 2    WREN: EEPROM Write Enable bit
         1 = Allows write cycles
         0 = Inhibits write to the EEPROM

bit 1    WR: Write Control bit
         1 = Initiates a write cycle. (The bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.)
         0 = Write cycle to the EEPROM is complete

bit 0    RD: Read Control bit
         1 = Initiates an EEPROM read. (RD is cleared in hardware. The RD bit can only be set (not cleared) in software.)
         0 = Does not initiate an EEPROM read

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
- n = Value at POR  '1' = Bit is set  '0' = Bit is cleared  x = Bit is unknown
## REGISTER 9-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS: 94h)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMP</td>
<td>CKE</td>
<td>D/Ä</td>
<td>P</td>
<td>S</td>
<td>R/W</td>
<td>UA</td>
<td>BF</td>
<td></td>
</tr>
</tbody>
</table>

**bit 7**
- **SMP**: Sample bit
  - **SPI Master mode**:
    - 1 = Input data sampled at end of data output time
    - 0 = Input data sampled at middle of data output time
  - **SPI Slave mode**:
    - SMP must be cleared when SPI is used in slave mode
  - **I²C Master or Slave mode**:
    - 1 = Slew rate control disabled for standard speed mode (100 kHz and 1 MHz)
    - 0 = Slew rate control enabled for high speed mode (400 kHz)

**bit 6**
- **CKE**: SPI Clock Edge Select (Figure 9-2, Figure 9-3 and Figure 9-4)
- **SPI mode**:
  - For CKP = 0
    - 1 = Data transmitted on rising edge of SCK
    - 0 = Data transmitted on falling edge of SCK
  - For CKP = 1
    - 1 = Data transmitted on falling edge of SCK
    - 0 = Data transmitted on rising edge of SCK
  - **I²C Master or Slave mode**:
    - 1 = Input levels conform to SMBus spec
    - 0 = Input levels conform to I²C specs

**bit 5**
- **D/Ä**: Data/Address bit (I²C mode only)
  - 1 = Indicates that the last byte received or transmitted was data
  - 0 = Indicates that the last byte received or transmitted was address

**bit 4**
- **P**: STOP bit
  - (I²C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
  - 1 = Indicates that a STOP bit has been detected last (this bit is '0' on RESET)
  - 0 = STOP bit was not detected last

**bit 3**
- **S**: START bit
  - (I²C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
  - 1 = Indicates that a START bit has been detected last (this bit is '0' on RESET)
  - 0 = START bit was not detected last

**bit 2**
- **R/W**: Read/Write bit Information (I²C mode only)
  - This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next START bit, STOP bit or not ACK bit.
  - **I²C Slave mode**:
    - 1 = Read
    - 0 = Write
  - **I²C Master mode**:
    - 1 = Transmit is in progress
    - 0 = Transmit is not in progress
  - Logical OR of this bit with SEN, RSEN, PEN, RCEN, or ACKEN will indicate if the MSSP is in IDLE mode.

**bit 1**
- **UA**: Update Address (10-bit I²C mode only)
  - 1 = Indicates that the user needs to update the address in the SSPADD register
  - 0 = Address does not need to be updated

**bit 0**
- **BF**: Buffer Full Status bit
  - **Receive (SPI and I²C modes)**:
    - 1 = Receive complete, SSPBUF is full
    - 0 = Receive not complete, SSPBUF is empty
  - **Transmit (I²C mode only)**:
    - 1 = Data transmit in progress (does not include the ACK and STOP bits), SSPBUF is full
    - 0 = Data transmit complete (does not include the ACK and STOP bits), SSPBUF is empty

---

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **n** = Value at POR
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **x** = Bit is unknown

---

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REGISTER 9-2: SSPCON: SYNC SERIAL PORT CONTROL REGISTER (ADDRESS 14h)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>WCOL</td>
<td>SSPOV</td>
<td>SSPEN</td>
<td>CKP</td>
<td>SSPM3</td>
<td>SSPM2</td>
<td>SSPM1</td>
<td>SSPM0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3-0</th>
</tr>
</thead>
</table>

**WCOL:** Write Collision Detect bit  
Master mode:  
1 = A write to SPPBUF was attempted while the I2C conditions were not valid  
0 = No collision  
Slave mode:  
1 = SPPBUF register is written while still transmitting the previous word (must be cleared in software)  
0 = No collision

**SSPOV:** Receive Overflow Indicator bit  
In SPI mode:  
1 = A new byte is received while SPPBUF holds previous data. Data in SSPSR is lost on overflow. In Slave mode, the user must read the SPPBUF, even if only transmitting data, to avoid overflows. In Master mode, the overflow bit is not set, since each operation is initiated by writing to the SPPBUF register. (Must be cleared in software.)  
0 = No overflow  
In I²C mode:  
1 = A byte is received while the SPPBUF is holding the previous byte. SSPOV is a "don't care" in Transmit mode. (Must be cleared in software.)  
0 = No overflow

**SSPEN:** Synchronous Serial Port Enable bit  
In SPI mode:  
When enabled, these pins must be properly configured as input or output  
1 = Enables serial port and configures SCK, SDO, SDI, and SS as the source of the serial port pins  
0 = Disables serial port and configures these pins as I/O port pins  
In I²C mode:  
When enabled, these pins must be properly configured as input or output  
1 = Enables the serial port and configures the SDA and SCL pins as the source of the serial port pins  
0 = Disables serial port and configures these pins as I/O port pins

**CKP:** Clock Polarity Select bit  
In SPI mode:  
1 = Idle state for clock is a high level  
0 = Idle state for clock is a low level  
In I²C Slave mode:  
SCK release control  
1 = Enable clock  
0 = Holds clock low (clock stretch). (Used to ensure data setup time.)  
In I²C Master mode:  
Unused in this mode

**SSPM3:** SSMPO: Synchronous Serial Port Mode Select bits  
0000 = SPI Master mode, clock = Fosc/4  
0001 = SPI Master mode, clock = Fosc/16  
0010 = SPI Master mode, clock = Fosc/64  
0011 = SPI Master mode, clock = TMR2 output/2  
0100 = SPI Slave mode, clock = SCK pin, SS pin control enabled.  
0101 = SPI Slave mode, clock = SCK pin, SS pin control disabled. SS can be used as I/O pin.  
0110 = I²C Slave mode, 7-bit address  
0111 = I²C Slave mode, 10-bit address  
1000 = I²C Master mode, clock = Fosc / (4 * (SSPADD+1))  
1011 = I²C Firmware Controlled Master mode (slave idle)  
1110 = I²C Firmware Controlled Master mode, 7-bit address with START and STOP bit interrupts enabled  
1111 = I²C Firmware Controlled Master mode, 10-bit address with START and STOP bit interrupts enabled  
1001, 1010, 1100, 1101 = Reserved

Legend:  
R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as '0'  
- n = Value at POR  
'1' = Bit is set  
'0' = Bit is cleared  
x = Bit is unknown
PIC16F87X

REGISTER 9-3:   SSPCON2: SYNC SERIAL PORT CONTROL REGISTER2 (ADDRESS 91h)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>GCEN</td>
<td>ACKSTAT</td>
<td>ACKDT</td>
<td>ACKEN</td>
<td>RCEN</td>
<td>PEN</td>
<td>RSEN</td>
<td>SEN</td>
<td></td>
</tr>
</tbody>
</table>

bit 7  
GCEN: General Call Enable bit (In I^2C Slave mode only)
1 = Enable interrupt when a general call address (0000h) is received in the SSPSR
0 = General call address disabled

bit 6  
ACKSTAT: Acknowledge Status bit (In I^2C Master mode only)
In Master Transmit mode:
1 = Acknowledge was not received from slave
0 = Acknowledge was received from slave

bit 5  
ACKDT: Acknowledge Data bit (In I^2C Master mode only)
In Master Receive mode:
Value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
1 = Not Acknowledge
0 = Acknowledge

bit 4  
ACKEN: Acknowledge Sequence Enable bit (In I^2C Master mode only)
In Master Receive mode:
1 = Initiate Acknowledge sequence on SDA and SCL pins and transmit ACKDT data bit.
Automatically cleared by hardware.
0 = Acknowledge sequence idle

bit 3  
RCEN: Receive Enable bit (In I^2C Master mode only)
1 = Enables Receive mode for I^2C
0 = Receive idle

bit 2  
PEN: STOP Condition Enable bit (In I^2C Master mode only)
SCK Release Control:
1 = Initiate STOP condition on SDA and SCL pins. Automatically cleared by hardware.
0 = STOP condition idle

bit 1  
RSEN: Repeated START Condition Enable bit (In I^2C Master mode only)
1 = Initiate Repeated START condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Repeated START condition idle

bit 0  
SEN: START Condition Enable bit (In I^2C Master mode only)
1 = Initiate START condition on SDA and SCL pins. Automatically cleared by hardware.
0 = START condition idle

Note:  For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I^2C module is not in the IDLE mode, this bit may not be set (no spooling), and the SSPBUF may not be written (or writes to the SSPBUF are disabled).

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
- n = Value at POR "1" = Bit is set  '0' = Bit is cleared  x = Bit is unknown