Outline
- Physical and logic design
- CAD tools
- Algorithms and heuristics
- Synthesis
- Design Methodologies
- Physical Design
- Placement and Routing
- Effect of Deep Submicron
- Backannotation

Digital Testing: Design Flow

Logic and Physical Design

CAD Tools
- All aspect of ASIC design depends on CAD tools
- CAD programs perform different tasks: Design entry, Simulation, Synthesis, layout, Test pattern generation, Floor planning, Technology mapping, Place and route, DRC, LVS, Parameter extraction
- Most these problems are NP-complete
- There is a need for algorithms that utilize some heuristic and a cost function to stop the computation.

Algorithms
- A recipe to solve a problem
- “Any well defined computational procedure that takes some values, as input and produces some values, as output.”
- The solution is valid most of the time
- Must be executed in reasonable time

Synthesis

Synthesis process according to representation level and tasks
**Synthesis**

High level synthesis flow:
1. System to RTL level
2. RTL to logic or register structure
3. Register to gate structure
4. Logic to gate structure
5. Structural to physical domain

**Comparing Synthesis Levels**

**Behavioral Domain**

**Structural Domain**

**Physical Domain**

**Comparing Design Levels**

**RTL Optimization**

**Multilevel Logic**

**Design Methodologies**

**Comparing Design Levels**
Semicustom Design

(a) Standard cells
(b) Gate arrays

Gate Arrays

A Gate Array 6-transistor cell

Patterned Cell

Metal
Diffusion
Poly

Routing

Interconnect resources in FPGA

Floor Planning

Various floor plans for the same chip

Floor Planning Perspective

Placement and Routing
**Mincut Approach to Placement**

(a) original

(b) final

(c) plan for iterative improvement

**Spanning Tree**

Global routing based on a spanning tree

**Back Annotation**

Two steps in back annotation:
- Netlist extraction
- Parameter extraction