Digital Testing: Boundary Scan Design

Objectives of The Chapter
- Traditional Board Testing
- Problems in testing PCB
- The origin of B-Scan
- Boundary-Scan architecture
- How does it work
- Modes of Operations
- External and internal testing
- TAP Controller: registers & instruction set
- BSDL

PCB Testing
- Traditionally: use of bed or nails
- Expensive
- Fragile
- Increase gate/pin ratio limit accessibility
- Fine trace between pins
- See trends in next slide

Trend in IC Growth

Why is Boundary-Scan?
- Originally 1985
  - DFT technique for board testing
  - To test connectivity between the ICs on the board
- Europe 1985: Joint Test Action Group
- USA 1990: IEEE 1149.1 Standard
- Very widely used at present

Boundary Scan Architecture
- A test access port (TAP) and 4 to 5 extra pins
  - Test Data Input (TDI)
  - Test Data Output (TDO)
  - Test Clock TCK
  - Test Mode Select (TMS)
- Group of registers
  - Instruction reg (IR)
  - Data reg (DR): Bypass, Boundary-Scan Reg, ID Reg
- TAP Controller
What is Boundary-Scan?

- Each I/O of the ICs on the board are registered through a Boundary-Scan flip-flops scan cell (BSC) attached to all PI/PO of the chips on the board.
- The results of the test are scanned out by connecting all the BSCs (boundary-scan register, BSR) in one daisy chain.
- A test access port (TAP)
- Four extra pins
- 16-state FSM Boundary-scan controller to manage the test data
- Follows standard IEEE 1149.1
- This DFT technique is independent of the scan design.

Traditional Board Testing

Traditional Test – Bed of Nails

Bed-of-nails in-circuit tester

Boundary-scan Architecture

Test Access Port: Registers
IEEE 1149.1 Device Architecture

- A set of four dedicated test pins
- Test Data In (TDI)
- Test Mode Select (TMS)
- Test Clock (TCK)
- Test Data Out (TDO) — and one optional test pin
- Test Reset (TRST*)

These pins are collectively referred to as the Test Access Port (TAP).

IEEE 1149.1 Device Architecture

- A boundary-scan cell, connected internally to form a serial boundary-scan register (Boundary Scan).
- A finite-state machine TAP controller with inputs TCK and TMS.
- An n-bit (n > 2) Instruction Register (IR), holding the current instruction for TAP.
- A 1-bit bypass register (Bypass).
- An optional 32-bit Identification Register (Ident) capable of being loaded with a permanent device identification code.
Instruction Register

- All the IRs of the IC are connected in a chain
- The appropriate instructions are shifted in serially
- The individual instructions are captured in parallel

The Instruction Register

- Using the Instruction Register (IR)

Using the Instruction Register (IR)

- TAP Controller
  - Responds to TMS signals at the positive edge of TCK
  - Controls the data and the instructions
  - Resets after five consecutive TMS

Test Access Port

- Bypass Register
  - Used to bypass the corresponding chip
  - The flow of the test data is as indicated by the heavy lines in the figure to the right
  - A one flip-flop register
  - Received the data from TDI and at the Capture DR state
Boundary-Scan Register

Only Capture and Shift no Update
Note: mandatory instructions do not require Update on input scan cells
Used on sensitive device inputs e.g. System Clock

Interconnect Test Example

Detecting any 2-net short circuit

The Instruction Set
- Three mandatory instructions
  - BYPASS, INTEST AND SAMPLE/PRELOAD
- Optional instructions:
  - IDCODE, INTEST, RUNBIST, CLAMP, HIGHZ
- Public and private instructions
- Private instructions need not be documented
- The instructions loaded through the chip TDI shifted in IR during Shift-IR state

Instruction Scan
Testing Internal Logic

- Use of an optional instruction, INTEST
- The test is applied through TDI
- Then shift out as in the case of EXTEST

Modes of Operation

- Normal Tap controller idle in Test-logic-Reset
- Select MUXes of flip-flops
- External Testing (EXTEST)
  - Shift DR, Update DR (latch at output)
  - Capture DR (at the output), Shift DR (through TDO)
- Testing internal logic (INTEST)
  - Shift DR, in data Update DR (apply to internal logic)
  - Capture DR (at the output), Shift DR (through TDO)
- Test the BSCAN Register

External Testing

- The output BSCAN Register is a representative of all such cells for the circuit
- The output BSCAN Register is also a representative of all cells
- The test signal is applied at the input and latched at the hashed flip-flops
- The output signal is now visible at the input of another cell

Capture the Stimulus

- Shift-DR: shift stimuli through TDI
- Stimuli intended for the internal logic
- Update-DR: apply the stimuli to the internal logic
Capture -DR: capture the respond at the output pins of the IC
Shift-DR: Shift out the results through the BSR toward TDO

Boundary-Scan Description Language
- BSDL is a subset of VHDL (VHSIC Hardware Description Language) that describes how IEEE 1149.1 is implemented in a device and how it operates.
- Entities in HSDL are used to describe modules as well as devices.
- A module is any level of architecture above the device level, including boards, multichip modules, backplanes, subsystems, and systems.
- In addition, HSDL provides two new packages used to indicate that an entity is an HSDL device or module.

Elements of BSDL
- Entity descriptions
- Generic parameter
- Logical port description
- Use statements
- Pin mapping(s)
- Scan port identification
- Instruction Register description
- Register access description
- Boundary Register description

Serial Vector Format (SVF)
- SVF is a standard ASCII format for expressing test patterns that represent the stimulus, expected response, and mask data for IEEE 1149.1-based tests.