A LOW POWER VOLTAGE BASED WINNER-TAKE-ALL CIRCUIT

FOR ANALOG NEURAL NETWORKS

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Abstract- This paper presents a voltage based CMOS winner-take-all (WTA) circuit for analog voltage signals. The WTA circuit is based on a winner follower and wide-range transconductance amplifiers. The voltage based design uses capacitive storage for low power consumption. The circuit is modularized and its layout size is a linear function of the number of inputs. This makes the circuit easy to be implemented in VLSI circuit. The circuit’s processing speed is accelerated by wide-range transconductance amplifiers which offer an extraordinary signal gain. Power consumption is reduced by shutting the transconductance amplifiers off after the competition is completed, while the processing results are stored in the capacitors of the WTA circuit. Schematic organization of this WTA circuit and computer simulation results are also presented.
I. INTRODUCTION

Analog circuit realization of neural networks may exhibit much higher performance than the digital equivalent. The design area and processing time can be much smaller than that of the corresponding digital circuit. Although analog computing is less precise than digital, this factor is not critical in neural network applications, where the results are expected to be less crispy, and where redundancy of the processing elements makes the results robust to the computational errors.

The winner-take-all (WTA) is an important circuit for neural network applications in which the most activated neuron has to be selected or a specific output obtained. There were several structures of WTA circuits proposed and they can be broadly categorized as the current based and the voltage based structure. The current based structures use the current signal as the carrier of information. They are easier to implement since the current signal can be added simply by wiring two signal lines together. Several developed structures [1], [2] have compact design area and show very good time performance. The existing voltage based structure [3], [4] are
slightly larger with comparable speed and power consumption. Voltage based structures have one potential advantage over current based designs. In current based structures, in order to sustain information, a current must flow dissipating the energy. In voltage based structure, the voltage can be maintained on capacitive storage elements practically without dissipating any energy, provided the leakage current is neglected.

This paper presents a voltage based CMOS WTA circuit which is fast and constructed by several identical cells. The basic structure of the WTA circuit is described in the Section II, and Section III presents its detailed implementation. Section IV presents the computer simulation results, and Section V is the conclusion.

II. THE WINNER FOLLOWER CIRCUIT

Fig. 1 shows a winner follower circuit with \( N \) nMOS transistors for \( N \) inputs signal \( V_{\text{IN}}^{[1]} \), \( V_{\text{IN}}^{[2]} \), ..,\( V_{\text{IN}}^{[N]} \). These transistor's drains are connected to the voltage supply \( V_{\text{DD}} \) and sources are connected to the load capacitor \( C_L \). Input signals \( V_{\text{IN}}^{[1]} \), \( V_{\text{IN}}^{[2]} \), ..,\( V_{\text{IN}}^{[N]} \) are connected to the transistors’ gates via input capacitors \( C \).

Assume that at the beginning of the competition the circuit had zero initial conditions, i.e. \( V_{\text{OUT}} = V_1 = V_2 = .. V_N = 0 \) at \( t = 0^- \). At \( t = 0^+ \) the input voltages were set, \( V_k = V_{\text{IN}}^{[k]} \), \( k = 1, 2 ..N \), and nMOS transistors, \( M_k \), \( k=1,2.. \) N, with \( V_k \) greater than threshold voltage \( V_{\text{th}} \) were turned on and began to charge \( C_L \) thus increasing the output voltage, \( V_{\text{OUT}} \). Any transistor \( M_k \) for which \( V_{\text{OUT}} > V_k-V_{\text{th}} \) would be cut off and would stop charging \( C_L \). For the total circuit, charging \( C_L \) ceases when \( V_{\text{OUT}} = \text{Max}\{V_k -V_{\text{th}} | \ k = 1,2, ..N \} \). In this scenario, \( V_{\text{OUT}} \) would raise and follow
the winner input with the largest \( V_k \). For this reason we call the circuit in Fig. 1 the winner follower.

The WTA circuit presented in the next section is based on the mechanism of the winner follower. Additional electronic pull-up and pull-down devices, such as differential amplifiers or transconductance amplifiers, can be used to aggregate the difference between \( V_{OUT} \) and \( V_k \)s. If \( V_k < V_{OUT} - V_{ih} \), \( V_k \) will be pulled down to the ground by the circuit, otherwise \( V_k \) will be pulled up to \( V_{DD} \). As a result, only the winner can survive the competition and go to a high voltage; the others are forced down to the ground.

III. CIRCUIT DESCRIPTION

The diagram of the proposed WTA circuit is shown in Fig. 2. It contains the winner follower structure enhanced by the feedback loops with transconductance amplifiers [6]. The schematic of a wide-range transconductance amplifier is shown in Fig. 3. This wide-range transconductance amplifier has two inputs, \( V_+ \) and \( V_- \). The output voltage is equal to \( V_O = A \left( V_+ - V_- \right) \) and the amplifier gain, \( A \), is very large which makes this amplifier very easy to saturate. If \( V_+ \) is slightly larger than \( V_- \), then \( V_O = V_{DD} \), and if \( V_+ \) is slightly less than \( V_- \), then \( V_O = 0V \). For this reason, using this wide-range transconductance amplifier not only can provide full range of output voltages but also it can enhance the resolution of the WTA circuit.

The combination of the winner follower and the wide-range transconductance amplifiers is shown in Fig. 4. In this WTA circuit, each competitor requires one cell. In each cell, the nMOS transistors \( M_1 \) and \( M_3 \) form an input buffer which makes the source voltage of \( M_1 \) follow \( V[k] - V_{ih} \). This reduces the input voltage of the winner to the level of the winner follower output and permits very high resolution of the competition process. Transistors \( M_2 \) and \( M_4 \) in each cell form
the winner follower with output $V_{\text{OUT}}$. In this circuit realization the original follower structure was enhanced by adding two nMOS transistors $M_3$ and $M_4$ with a low gate voltage $V_G=0.1V$. With this gate voltage $M_3$ and $M_4$ work like current sources which drain the excessive charge to the ground to prevent the charge accumulation at the sources of $M_1$ and $M_2$. The wide-range transconductance amplifier in "Cell k" takes $V_{\text{OUT}}$ and $V^{[k]}-V_{\text{th}}$ as inputs and amplifies the difference between $V^{[k]}-V_{\text{th}}$ and $V_{\text{OUT}}=\max\{V^{[k]}-V_{\text{th}}, k=1,2,..,k,..\}$. The outputs of the wide-range transconductance amplifiers are fed back to $V^{[k]}$ to provide a positive feedback that accelerates the changes of $V^{[k]}$. If $V_{\text{IN}}^{[k]}$ is the winner, $V^{[k]}$ will be pulled up to $V_{\text{DD}}$ and all other input voltages will be pulled down to the ground. At the end of the competition all transconductance amplifiers can be shut down by setting the bias voltage $V_b$ to zero. This will reduce the power consumption when the WTA circuit completes its work.

IV. COMPUTER SIMULATION RESULTS

The computer simulation of the presented WTA circuit uses Pspice, -Design Center$\textregistered$ Software of MicroSim Corporation. The circuits are simulated in $2\ \mu\text{m}$ CMOS technology with level 3 nMOS and pMOS transistor models. In the simulation all transistors were set to have the same $\beta$ value. According to the transistor model specifications, all nMOS transistors except $M_2$s in Fig. 4 have $W/L = 2\ \mu\text{m}/2\ \mu\text{m}$ and all pMOS transistors have $W/L=6\mu\text{m}/2\mu\text{m}$. $M_2$s gate geometric were set to $W/L = 4\ \mu\text{m}/2\ \mu\text{m}$ to enhance the real time performance of the winner follower. Although this modification would increase the capacitance load of the wide-range
transconductance amplifiers, the winner follower can raise faster to keep pace with the increasing
winner input, which improves the performance of the total WTA circuit.

Fig. 5 shows the simulation results of the time domain transient responses of $V^{[k]}$s in a
WTA circuit that contains 10 cells with $[V_{\text{IN}}^{[1]}, V_{\text{IN}}^{[2]}, \ldots, V_{\text{IN}}^{[10]}] = [0.5\text{V}, 2.6\text{V}, 2.65\text{V}, 2.7\text{V},
2.55\text{V}, 2.4\text{V}, 2.65\text{V}, 1.52\text{V}, 2.3\text{V}, 2.45\text{V}]$. Since $V_{\text{IN}}^{[4]}$ is the winner, $V^{[4]}$ was pulled up to its
highest value at 8ns and both the next largest signals, $V^{[3]}$ and $V^{[7]}$, were pulled down to the
ground at 12ns. The competition was finished in 12ns and the peak current was 4mA with the
average current during the competition period about 2mA. The obtained resolution of the WTA
is 50mV.

V. CONCLUSION

The proposed WTA circuit uses voltage signals to for its input and output information.
Since the competition result can be stored on the input gate capacitance, the power hungry wide-
range transconductance amplifiers can be shut down after the competition is over in order to
reduce total power dissipation. The circuit's connection complexity and layout area are both
linear functions of the number of competitors. With its modular design, simple connections, and
power saving scheme, the proposed WTA circuit is suitable for the VLSI implementation.
REFERENCES


Fig. 1 The winner follower circuit.

Fig. 2 WTA circuit organization.

Fig. 3 The schematic and symbol of the wide-range transconductance amplifier.

Fig. 4 The modularized and linearly connected WTA circuit.

Fig. 5 The time domain transient response $V^{[k]}$. 