**INTRODUCTION**

What is Testing?

How Much is Enuf?

**Definition of Testing**

A part fails to operate properly
- Design does not correspond to specification
  - Logic design incorrect
  - Physical design incorrect
- Physical part does not correspond to design
  - Manufacturing defect present
  - Wear out defect present
- External or environmental disturbance
  - Transient disturbance
  - Power or temperature specification violated

**Outline**

- Reliability and testing
- Design process
- Verification & testing
- Faults and their detection
- Fault coverage
- Types of tests
- Test applications
- Design for Test
- Test economics

**Reliability and Testing**

- Reliability of electronics systems is no longer limited to military, aerospace or banking
- Used by almost everyone in the workplace
- Applied to smaller and smaller devices
- Have continually new failure modes
- Reliability depending on being error free
- Failures in both software and hardware
- Here we concentrate on hardware
The goal over time is to reduce the cost of manufacturing the product by reducing the per-part recurring costs:

- Reduction of silicon cost by increasing volume and yield, and by die size reduction (process shrinks or more efficient layout).
- Reduction of packaging cost by increasing volume, shifting to lower cost packages if possible (e.g., from ceramic to plastic), or reduction in package pin count.

Test Objective

Testing a circuit prior to fabrication is known as design verification. Verification is certainly done at various stages of the design process. Most viable design verification is through simulation. Testing is identifying that the fabricated circuit is free from errors. Need to specify what errors testing is looking for.
Types of Physical Faults

- Physical failures are manifested as electrical failures and are interpreted as faults on the logic level.
- Several physical defects may be mapped into few fault types.
- The main fault type is Stuck-at Fault.
- A fault is detected by a test pattern.
- Test pattern is an input combination that confirms the presence of the fault.

Faults and their Detection

Types of Logic Failures

- Specification
  - Behavioral or Register Transfer
  - Table of Combinations – Boolean Function
  - Sequential Circuit or State Machine Flow Table
  - Simulation Vectors and Responses
  - Informal Word Description of Functionality
- Verification Technique
  - Synthesis
  - Matching of Two Design Paths
  - Simulation – Emulation
  - Formal Verification

DFT Cycle

- **DFT Cycle**
  - RTL Description
  - Logic DFT Synthesis
  - Test Pattern Generation
  - Fault Identification
  - Fault Analysis
  - Fault Resolution
  - Functional Verification
  - Production Test

OUTLINE

- **DFT Cycle**
  - Testing Definition
  - Design Verification
  - Types of Tests
  - Implicit Testing
  - Explicit Testing
  - Production Test
  - Experiments and Quality Models
Possible Defects

- Two technologies, two physical defects map into the same stuck-at zero fault
- Notation used - A SA0, or A/0

Detecting Stuck-at Faults

Inputs | Fault Free Response | Faulty Response
--- | --- | ---
AB | A/0 | B/0 | Z/0 | A/1 | B/1 | Z/1
00 | 0 | 0 | 0 | 0 | 0 | 0 | 0
01 | 0 | 0 | 0 | 0 | 1 | 0 | 1
10 | 0 | 0 | 0 | 0 | 0 | 1 | 1
11 | 1 | 0 | 0 | 0 | 1 | 1 | 1

Sequential Circuit

Inputs | FF Response | Faulty Response
--- | --- | ---
SR | A/0 | S/0 | R/0 | A/1 | S/1 | R/1
01 | 0 | 0 | 0 | X | 0 | 0 | 0
10 | 1 | 1 | 0 | 0 | 1 | 1 | 1
11 | 0 | 0 | 1 | 1 | 1 | 1 | 1

Outline

- Testing Definition
- Design Verification
- Types of Tests
- Implicit Testing
- Explicit Testing
- Production Test
- Experiments and Quality Models
Types of Testing

- Exhaustive test used to detect the faults on a 2-input AND gate is not practical for circuits with 20 or more primary inputs.
- Pseudo-exhaustive: exhaustive for components in the circuits, segmentation or partitioning.
- A random test is also viable to detect faults, but pseudo-exhaustive tests are more realistic for Stuck-at Faults.
- Deterministic or fault oriented tests.

Types of Tests

Functional Testing

- Exhaustive & pseudo-exhaustive testing:

  Partial dependence circuits:
  - A circuit in which no primary outputs (PO) depend on all the primary inputs (PI).
  - Each output tested using $2^n$ inputs. ($n_i < n$ shows inputs affecting PO).

Example:

Exhaustive & pseudo-exhaustive testing

Example:

Exhaustive & pseudo-exhaustive testing

Example:

Consider the following circuit:

Example:

Consider the following circuit:
Functional Testing

Example: the following shows 8 input vectors to test exhaustively h.

<table>
<thead>
<tr>
<th>a</th>
<th>b</th>
<th>c</th>
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Functional Testing

Example: Add vectors 5 - 8 to test exhaustively g and 9 - 10 to test exhaustively y.

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Functional Testing

Example: Add missing combinations to vectors 4 and 9 to test exhaustively x.

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Pseudo Random TPG: an LFST

Chip defects are cause by the circuitry or the package.

A common approach is an LFST or an LFT.

Each chip has a limited number of bits and a limited time to test.

The test program is designed and then applied to the chips.

The test result is used to determine if the chip is acceptable.

A common test board is the Manufacturing Test Board.

The chip will be assembled on the test board.

Each chip has a limited number of bits and a limited time to test.

The test program is designed and then applied to the chips.

The test result is used to determine if the chip is acceptable.

A common test board is the Manufacturing Test Board.
Testing for wear out and transient defects

- On-line testing
  - Embedded checkers – error detection
  - Periodic diagnostic programs
  - Watchdog checkers
- Repair or diagnostic test

IMPORTANT OBSERVATION
Part can Operate Correctly with a Defective Component

- Detect isn’t Bad Enough to Prevent Correct Operation
  - CMOS gate-oxide short
  - low R...
  - Can Cause Intermittent Errors
- Component is Redundant

MAJOR TESTING CATEGORIES

IMPLICIT
- On-Line Test for Run-time Errors
  - Concurrent Checking, Monitoring, Built-in Test

EXPLICIT
- Off-line test for permanent defects

OUTLINE

- Testing Definition
- Design Verification
- Types of Tests
- Implicit Testing
- Explicit Testing
- Production Test
- Experiments and Quality Models

IMPLICIT TESTING
- Concurrent Checking, Monitoring, On-Line Test, Built-in Test
- Test of operational system - Normal system inputs
- Errors detected as they occur
- Temporary as well as permanent faults
- Identifies failed units for repair

CIRCUIT LEVEL TECHNIQUES
- Hardware faults detected
- Prevents undetected data errors

SYSTEM LEVEL TECHNIQUES
- In Addition, Detect Control and Software Faults
**Off-chip and on-chip Test**

**Application**

- Off chip: requires **expensive testers**
- On chip: uses the **embedded testing** technique
- On chip may also be done during normal operation of the circuit: **on-line testing**

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**On Line Testing**

![Diagram of Circuit Under Test](image)

**On- vs Off-Chip Testing**

![Diagram comparing high and low bandwidth](image)

**Explicit Testing**

- Off-line test for permanent faults
  - Special test inputs used

- **OUTPUT RESPONSE ANALYSIS**
  - Stored Response
  - Comparison (gold unit)
  - Compact Testing
    - Signature Analysis (LSFR)

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**OUTLINE**

- Testing Definition
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**EXPLICIT TEST TECHNIQUES**

- **Parametric Test**
  - Measure or "threshold" analog parameters
  - DC — Voltage levels, drive current, power,...
  - AC — Rise, fall, delay times

- **Boolean Test**
  - Digital test of logic operation
  - Also called **functional test**

- **Quasi-Boolean Test (AC test)**
  - Delay Fault Test
TESTERS COST OVER $1 000 000

Resources applied on a typical tester:
- Memory blocks
- Various clocks
- Power supplies
- AD and DA converters
- Current measurement
- Frequency converters

EXPLICIT TESTS ACCORDING TO PURPOSE
- Characterization Test
- Production or Manufacturing Test
- Reliability (Accelerated Life) Test
- Stress Screen (Burn-In) Test
- Acceptance or Incoming Inspection
- Quality Test
- Repair, diagnosis, fault location

OUTLINE
- Testing Definition
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PRODUCTION OR MANUFACTURING TEST
- Test of Manufactured Parts
  - Sort Out Defective Parts
  - Bin Parts for Different Specifications
- Chip
  - Wafer Sort or Probe
  - Test Site
  - Die
  - Burn In
  - Final Package
- Board
  - Bare Board
  - In-Circuit or Bed-of Nails
  - Functional or Edge Connector

RELIABILITY (ACCELERATED LIFE) TEST
- Test to Estimate Time to Failure in Normal Operation
  - Part is Tested After High Temperature Stress

ACCEPTANCE OR INCOMING INSPECTION
- Test to Determine Degree of Compliance with Purchaser’s Requirements
QUALITY TEST
- Sample of Each Lot Tested
- Used by Quality Assurance Department
- Estimates Quality Level of Manufactured Parts

REPAIR, DIAGNOSIS, FAULT LOCATION
- Test to Locate Failure Site on Failed Part
  - Board or boards in system
  - Chip or chips on board
  - Not on chip
- Purpose
  - Return system or board to correct operation
  - Improve chip yield, reliability, quality

REPAIR, DIAGNOSIS, FAULT LOCATION
- Hardware Diagnosis Techniques
  - Direct observation
    - place chip in failed state
    - observe image
    - light emission
    - thermal effects
    - focused electron beam interaction
  - Measure chip response to outside physical stimulus
    - scan chip with laser, electron beam, ion beam
    - monitor chip I/O, power supply
- Limitations
  - Defect dependent
  - some defects don’t emit light or cause heating
  - Needs access to chip transistors and internal wiring

PRODUCTION TEST

DEFINITIONS
- Quality Level, QL
  - Fraction of Parts Passing Test that are Good
- Defect Level, DL = 1 - QL
  - Fraction of Parts Passing Test that are Bad
    - Measured in DPM, Defects per Million
    - Typical Claim is Less than 200 DPM (0.02%)
- Yield, Y
  - Fraction of Manufactured Parts that are Good
    - Typically 10 to 90%
- Reject Ratio
  - Fraction of Manufactured Parts that Fail Test
    - Used to Estimate Yield
TEST THOROUGHNESS

Measured by:
- Test transparency, TT
  - Fraction of Defects NOT Detected by Test
  - Estimated by FAULTS Missed by Test
    Faults are Logical Models of Defects
- Required Test Transparency
  - Depends on Yield and Acceptable Quality Level

ESTIMATING BOARD QUALITY LEVEL

- N Components per Board
- Component Defects are identical and independent
- Each Component has Probability q of being defective
- Probability that Board has no Defective Component is:
  \[ P = (1 - q)^N \]

<table>
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<th>DL</th>
<th>q</th>
<th>P (%)</th>
<th>1 - P</th>
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<td>66.9%</td>
<td>33.1%</td>
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<td>96.6%</td>
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<td>200</td>
<td>100 DPM</td>
<td>0.01%</td>
<td>98.8%</td>
<td>1.2%</td>
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OUTLINE

- Testing Definition
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Test Economics

- The life cycle of a product is shorter than its design cycle
- Time to market needs to be shorten
- Testing is necessary for reliability and for improving yield
- Disciplined design to facilitate testing is known as Design for Test (DFT)

Time to Market

![Graph showing Time to Market and Loss of Revenues]

Yield and Fault Coverage

![Graph showing Yield and Fault Coverage]

Loss of Revenues

Time to Market

Time in Months

Defect Level

Fault Coverage

Revenues
**Yield and Defect Level**

**Defect Level**

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<td>0.1</td>
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<td>0.025</td>
<td>0.0125</td>
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**Yield and Defect Level**

**WAFER SORT**

- Gross Test:
  - Test for Gross Defects - Idd, Pin Leakage,...
- Parametric Test:
  - Measure analog parameters of device
  - DC - Voltage levels, drive current, power,...
  - AC - Rise, fall, delay times
- Boolean Test:
  - Digital test of Logic Operation
  - Called Functional Test by Chip Testers
  - Based on Fault Model

**WAFER SORT (AKA WAFFER PROBE, PROBE TEST)**

- Y, Yield = Fraction of die passing test
- Y_D = Die Yield
- Y_B = Gross Yield
- Y_P = Boolean Yield

**BOOLEAN QUALITY LEVEL DEPENDENCE ON Y AND TT**

**THEOREM:**

The Boolean Quality Level achieved by a test with Boolean Test Transparency, TT, for a process of Boolean Yield, Y, is given by:

\[ QL = Y^T_T \]

**COROLLARY:**

For Tests that Result in Defect Levels, DL, less than 1000 DPM this can be simplified to:

\[ DL = (1 - Y) T_T \]

and further simplified for Y > 90% to:

\[ DL = (1 - Y) T_T \]

**MOTOROLA 6802 WAFFER SORT EXPERIMENT**

- Gross: 18.5
- Boolean: 7
- Parametric: 12
- Pass: 18.5
- Fail: 4

Single Stuck-Fault Coverage = 99.3%

\[ Y_B = 12 / 18.5 = 65.167\% \]

\[ Y_0 = 18.5 / 22.5 = 82.2\% \]

**REQUIRED TT AND C FOR DL = 200 DPM.**

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**Test transparency**

**Fault coverage**