Digital Testing: Current Testing

Outline
- Why current testing
- Effect on propagation delays
- Measurement of current
- Test pattern generation
- Subthreshold current
- Effect of deep submicron

What is Current Testing
- Also called IDDQ Testing
- Measurement of the supply, \( V_{DD} \), quiescent current
- the sum of all off-state transistors
- Useful only for CMOS circuits
- Limitation due to shrinking technology

Current Testing Basics
- CMOS circuits operate with normally negligible static current (power)
- But, a defect that causes an appreciable static current can be detected by measuring the supply current, \( I_{DDQ} \)
- Technique used since inception of CMOS technology
- Limitation due to shrinking technology

IDDQ Testing
- IDD --- Current flow through VDD
- \( Q \) --- Quiescent state
- IDDQ Testing --- Detecting faults by monitoring IDDQ

Advantages of IDDQ Testing
- Fault effect is easy to detect
- Many realistic faults are detectable
- ATPG is relatively simple
- Test length is shorter
- Built-in current sensing is possible

CMOS circuit

Inputs

Outputs

Normal IDDQ: \( \sim 10^{-9} \) Amp.
Abnormal IDDQ: \( > 10^{-5} \) Amp.
Inductive Fault Analysis (IFA)

- A systematic method to generate realistic fault lists
- Taking into account:
  - Circuit fabrication technology
  - Defect statistics
  - Physical layout

Calculation of Defect Likelihood

Whether a fault presents depends on:
1. Size of spot (defect statistics)
2. Distance of two conductors (layout)
3. Fabrication process

 IDDQ Distribution

\[(M_d - M_g)\] should be an easily measurable quantity

How Does it Work?

- Apply a test pattern
- Wait for the transient to settle down
- Measure the current

Needed:
- How to generate the patterns
- How to measure the current
- But, first current characteristics

Dynamic Current

Inverter: Good and Faulty \(I_{DDQ}\)
A NAND Tree

- Measurement requires the current settling down.
- Circuit to show the effect of the delays shown on the next slide.

Current for the NAND Tree

IDDQ Measurement

- Measurement may interfere with the measured current.
- A successful measurement should be:
  - Easily placed between the CUT and the bypass capacitor of the power pin.
  - Capable of measuring small currents.
  - Non-intrusive, no drop of VDD.
  - Fast measurement few ns per pattern.
- Two types: on- and off-chip.

External Measurement

Current Sensing Structures

- BICS based on Bipolar Transistor and Differential Amplifier (Maly, ICCAD ’88).

When large IDDQ exists, V>V_R and fail flag is set.
- The switching circuit may switch off a faulty module to prevent large power consumption.
### Internal Measurement

![Internal Measurement Diagram](image)

**VDD-GND Shorts**
- Bridging Faults
- Gate oxide pinholes
- Floating gate & junction leakages

**Analysis of a Short**

For the shorted pMOS transistor, find:
- a path from $V_{DD}$ to $GND$ through this transistor,
- then $AB = 11$ is needed to detect this short using $I_{DQ}$

### Detecting Short Faults

![Detecting Short Faults Diagram](image)

**Test Pattern Generation (TPG)**

- Mainly two methods:
  - based on switch level using graph representation as for layout
  - based on leakage fault models

### Graph or Switch Based TPG

- Path A,B to test shorts on A transistors
- Path B,A to test shorts on B transistors

### Leakage Fault Model

- Assuming all possible shorts between the four nodes, bulk, source, gate, and drain results in 6 tuples
- The pattern is the conjunction of In & Out
- Some combinations are impossible: 00, 11
- To simplify, the 6 tuples are represented in octal number as shown in column N of the table
- The notation is used to characterize a 2-input NAND
- For instance for I/O=10 transistor fault code is N=43, $I_{DDQ}$ and represents the following faults: bg, gd, ps
Characterizing a NAND

Octal fault vector code for each transistor:

<table>
<thead>
<tr>
<th>X</th>
<th>N1</th>
<th>N2</th>
<th>P1</th>
<th>P2</th>
</tr>
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<tbody>
<tr>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>0</td>
</tr>
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<tr>
<td>4</td>
<td>43</td>
<td>26</td>
<td>26</td>
<td>26</td>
</tr>
</tbody>
</table>

I/O octal code, eg.: 6=110=5 A=1, B=1, O=0

Impact of Deep Submicron

- Deep submicron transistors work at lower $V_t$
- The lower $V_t$ the higher $I_{DDQ}$
- The discrepancy between the faulty and non-faulty $I_{DDQ}$ is narrowing

Controlling $I_{DDQ}$

- Reverse biasing the substrate
- Cooling the devices
- Using dual threshold voltage
- Partitioning the circuit to manageable $I_{DDQ}$

Change of Current with Body bias and Temperature

- $I_{DDQ}$ with input state of 0
- $I_{DDQ}$ with input state of 1
- Normalized $I_{DDQ}$ to $I_{DDQ}$ of 0.18um Gate at 150C without Body Bias
- $L_g=.18u$ at 150C
- $L_g=.25u$ at 150C
- $L_g=.18u$ at 25C
- $L_g=.25u$ at 25C
- $L_g=.18u$ at -50C
- $L_g=.25u$ at -50C

Source or Drain Break Faults

- In a gate
- May drift to intermediate voltage

Stuck-open Faults

A B C D O
T1 = 1 1 1 1 0
T2 = 0 0 0 1 ?

When T2 is applied, charge sharing among x, y and o occurs, hence may draw a large current in the inverter.
Other Faults That Can Be Detected

- Gate-oxide short (Hawkins ITC85, D&T 86)
- Most stuck-at faults (Fritzmeyer ITC-90)
-Latch-up
- Delay faults
- Any other fault due to extra conductor, missing isolating layer, excess well/substrate leakage, etc.

Circuit Constraints

To ensure IDDQ detectability, two conditions must be satisfied:
1. Normal IDDQ must be small
2. Faults must result in large IDDQ

A Good Circuit That May Be Identified As Being Faulty

When the third pattern AB=10 is applied, change sharing between x, z occurs, and a large current may exist in the inverter. However the output is still correct. Problem due to high impedance node

A BF That Cannot Be Detected By IDDQ

ϕ=1: a=0, b=1 ϕ=1: Eventually x=y (as one signal will dominate), no big current
Problem due to feedback loop

Problems with Dynamic Logic

Problems:
1. Large current in normal circuits due to charge sharing
2. Very few faults are detected because of the precharge property (no direct path VDD-GND)
3. Fault masking of BF(a, b) due to BF(o, p)

Transistor Group

Transistor group (TG) --- "Channel-connected component"
Connections between two TGs are unidirectional
Control direction or loop can be defined
A Minimum Set of Design & Test Rule for IDDQ Testing (Lee FCAD’92)

A1. Gate and drain (or source) nodes of a transistor are not in the same TG.
A2. No conducting path exists from VDD to GND during steady state.
A3. Each output of a TG is connected to VDD or GND during steady state.
A4. No control loops among TGs exist.
A5. The bulk (or well) of an n-/p-type transistor is connected to GND (VDD).
A6. During testing, each PI is controlled by a monitored power source.

Results of Design & Test Rules

Theorem 1: All irredundant single BFs in a circuit satisfying A1-A6 can be detected using IDDQ testing.

Theorem 2: For a circuit satisfying A1-A6, a test detecting a single BF also detects all multiple BFs that contain f.

Theorem 3: If any one of A1-A6 is removed, then circuits exist for which IDDQ testing cannot give correct test results. Strategies for dealing with circuits not satisfying each rule are required to ensure IDDQ detectability.

Fault Simulation

1. Fault models — Bridging, break, stuck-open, stuck-at?
2. Fault list generation — need inductive fault analysis
3. Fault coverage?
4. Easy for bridging and stuck-on faults
5. Difficult for break and stuck-open faults
6. Stuck-at faults may or may not be modeled as short to VDD or GND

Fault simulation for BFs

If A1-A6 are satisfied, then fault simulation is quite simple

1. Perform a good circuit simulation for the given test pattern.
2. Any BF between a node with logic 1 and a node with logic 0 is detected.

No simulation on faulty circuit is needed.
No fault list enumeration is needed.

Test Generation

1. Conventional test generation for stuck-at faults can be modified to detect BFs.
2. No fault propagation.
3. Must make sure the faults result in a conducting path between VDD and GND. Switch level test generation may be necessary.
4. Break and stuck-open faults are difficult to detect.

Test generator for BFs

Again, assume A1-A6 are satisfied

1. For the BF (a, b) to be detected, add an XOR gate with its inputs connected to a and b.
2. The test generator work is simply to set the output of the XOR gate to be 1.

No Fault propagation.
Current monitoring Techniques

External Devices (Hawkins 86, 89)

Problems:
1. Current resolution is limited.
2. Test equipment must be modified.
3. Current cannot be measured at the full speed of the tester.

Built-in Current Sensors (BICSs)

QTAG $I_{\text{DDQ}}$ Monitor (Baker, ITC '94)

Current sensing in the interface

Built-in Current Sensors Based on Logic Threshold

Improvement on Favalli’s design...

Merge all MT and MTD respectively
Using BiCMOS design

Improvement on Fayalli’s Design

BICS Based on Integrators

Miura & Kinoshita (ITC-92)

level translator converts the input high (low) voltage V to a logic 0 (logic 1) at x

Fault effect can be accumulated through several clock cycles

BICS Based on Dual Power Supply & Operational Amplifier

BICS Based on Current Conveyor

Advantages of Built-In Current Sensors (BICS)

• Higher test rate compared to external devices
• Easier to partition circuits
• Easier to control current resolution
• Suitable for mixed-mode circuits
• Built-In self test capability achievable
• Lower test equipment cost
• On-Line testing possible

Verhelst’s BICS Patent

output O1 of the op-amp.
A1 adjusts the gate voltage of T6.
IDD is mirrored to T1 for current comparison in CMP

VDD = 3V

Virtual Short
Current Mirror

virt - VDD

Iz ~ Ix

Iy

CUT

Fail/Pass

Threshold Detector

Virtual short
Current Conveying

VDD - VDD'

Iy ~ Ix

Virtual Short

Virtual Short

BICS Based on Current Conveyor

Advantages of Built-In Current Sensors (BICS)
Disadvantages of BICS

- Impact on circuit performance
- Reliability of itself
- Area overhead
- Power consumption